This listing of claims will replace all prior versions, and listings, of claims in the application:

In the Claims:

Claims 1-18 (canceled)

19. (original) An integrated circuit including a phase lock loop circuit comprising:

a clock input terminal for accepting a clock signal;

a phase/frequency detector (PFD) circuit including a clock input connected to receive the clock signal and including a feedback input for receiving a PFD feedback signal and including a PFD output for providing a PFD output signal;

a first charge pump (CP) circuit including a first CP input connected to receive the PFD output signal and including a first CP output for providing a first CP output signal;

at least one external feedforward output terminal connectable to couple at least one of the PFD output signal and a CP output signal to an external loop filter;

a loop filter (LF) including a filter input connected to receive the first CP output signal and including a LF output for providing a LF output signal;

a loop controlled signal source (LCSS) including a LCSS input connected to receive a LF output signal and including a LCSS output for providing a LCSS output signal; and

a feedback circuit connected between the LCSS output and the PFD feedback input, the feedback circuit including;

an external feedback input terminal;

selector circuitry including a first feedback selection input connected to receive the LCSS output signal and including a second feedback selection input and including a selection output for providing a selection output signal;

a programmable program counter (PC) including a PC input connected to receive the selection input signal and including a PC output connected to provide a PFD feedback signal to the PFD feedback input;

a programmable swallow counter which includes a swallow counter input connected for receiving the PFD feedback signal and which includes a swallow counter output for providing a prescaler control signal; and

a programmable prescaler counter including a control input connected to receive the prescaler control signal and including a feedback input connected to receive a signal from the external feedback input terminal and including a prescaler output connected to provide a prescaler signal to the second feedback selection input.

20. (original) The integrated circuit of claim 19 further including:

a programmable reference counter connected to adjust the clock signal frequency and including an input connected to the clock input terminal and an output connected to provide the frequency adjusted clock signal to the PFD clock input.

21. (original) The integrated circuit of claim 19,

wherein the selector circuit includes an other external feedback input; and further including:

a bypass connection between the external feedback input terminal and the other external feedback input of the selection circuit, the bypass connection bypassing the programmable prescaler counter.

22. (original) The integrated circuit of claim 19 further including,

a first external bias terminal;

a second external bias terminal; and

a selector circuit connecting the first charge pump output to the LF and to an external feedforward output terminal; and

wherein the first CP is interconnected with the first and second external bias terminals;

23. (original) The integrated circuit of claim 19 further including:

a second charge pump (CP) circuit including a second CP input connected to the PFD output and including a second CP output; and

wherein the second CP output serves as an external feedforward output terminal.

Claims 24-26 (canceled)